Welcome to

Conference
January 28–30, 2025
Santa Clara Convention Center

Expo
January 29–30, 2025

SPEAKERS

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Zhiping Yang is the CEO of PCB Automation Inc. (https://pcbauto.ai) and an adjunct professor at Missouri S&T EMC laboratory. He worked in Waymo, Google, Apple, Cisco, and Nuova systems on automotive, consumer, and datacenter products. His research interests include signal integrity and power integrity methodology development for Die/Package/Board co-design, high-speed optical module, various high-speed cabling solutions, high-speed DRAM/storage technology, and high-speed serial signaling technology. He has published more than 70 research papers and 20 patents. His research and patents have been applied in Apple iPhone 5S/6/6S, Cisco UCS, Cisco Nexus 6K/4K/3K, and Cisco Cat6K products. He is actively involved with the IBIS Open Forum as a BoD member and officer. He is an IEEE Fellow and served the Technical Advisory Committee leadership roles in IEEE EMC society. He obtained his Ph.D. from University of Missouri-Rolla and his B.S. and M.S. from Tsinghua University, Beijing.

Ravi NarayaSwami, *Design Engineering Group Director, Cadence* rswami@cadence.com

Ravi NarayanaSwami is a Design Group Director in the Cadence Silicon Solutions Group with around 25 years of semiconductor development and systems engineering experience in Silicon Valley. His team's responsibilities include post-silicon tapeout activities to product validation related to high-speed SerDes and UCIe™ subsystem IPs. He holds an M.S.E.E from the Florida Institute of Technology.

UCIe Overview

Outline

- UCIe™ Channel Compliance Overview
  - Eye Diagram Requirement
  - Voltage Transfer Function (VTF)

Channel Spec: Eye Diagram Requirement\

Figure 5-15. Example Eye diagram

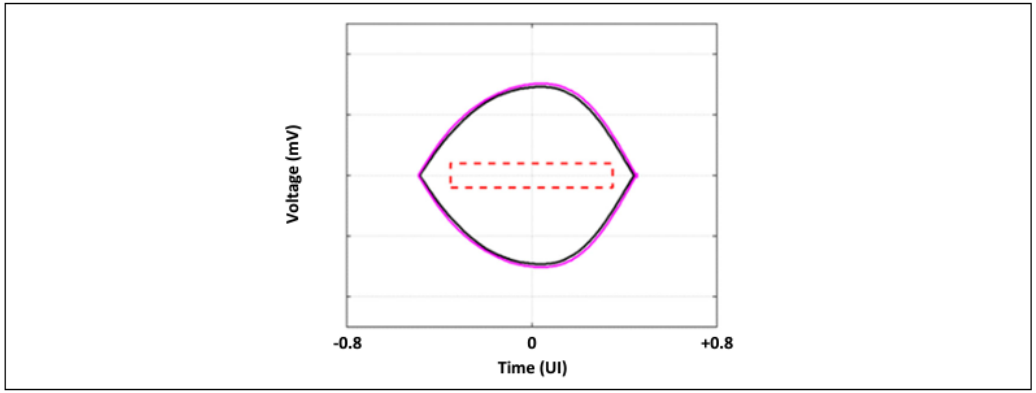


Table 5-10. Eye requirements

Data Rate (GT/s)	Eye Height (mV)	Eye width (UI)
4, 8, 12, 16[a c]	40	0.75
24, 32[a b c]	40	0.65

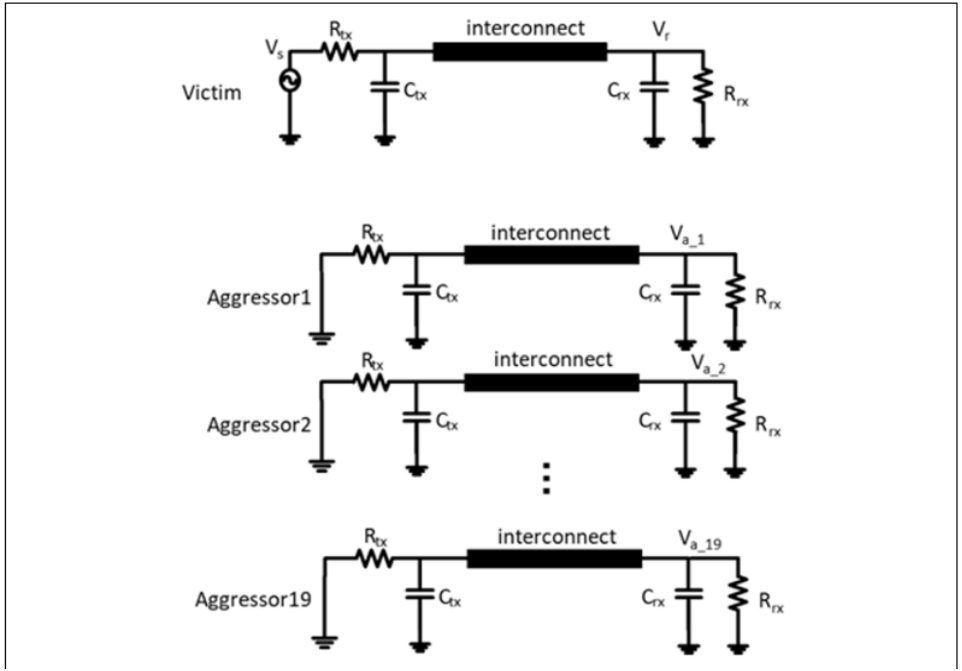
a. Rectangular mask.
b. With equalization enabled.
c. Based on minimum Tx swing specification.

Source: Universal Chiplet Interconnect Express Consortium (UCIe™). Refer to the UCIe™ specification for additional info.

Channel Spec: Voltage Transfer Function

Voltage Transfer Function (VTF) based metrics are used to define insertion loss and crosstalk. VTF metrics incorporate both resistive and capacitive components of TX and RX terminations. Figure 5-17 shows the circuit diagram for VTF calculations.

Figure 5-17. Circuit for VTF calculation



Source: Universal Chiplet Interconnect Express Consortium (UCIe™). Refer to the UCIe™ specification for additional info.

Channel Spec: VTF Loss

VTF loss is defined as the ratio of the Receiver voltage and the Source voltage, as shown in Equation 5-1 and Equation 5-2.

Equation 5-1.

$$L(f) = 20\log 10\left|\frac{V_r(f)}{V_s(f)}\right|$$

Equation 5-2.

$$L(0) = 20\log 10\left(\frac{R_{rx}}{R_{tx} + R_{channel} + R_{rx}}\right)$$

L(f) is the frequency dependent loss and L(0) is the DC loss. For unterminated channel, L(0) is effectively 0.

Source: Universal Chiplet Interconnect Express Consortium (UCIe™). Refer to the UCIe™ specification for additional info.

Channel Spec: VTF Crosstalk

VTF crosstalk is defined as the power sum of the ratios of the aggressor Receiver voltage to the source voltage. 19 aggressors are included in the calculation. Based on crosstalk reciprocity, VTF crosstalk can be expressed as shown in Equation 5-3.

Equation 5-3.

$$XT(f) = 10\log 10\left(\sum_{i=1}^{19}\left|\frac{V_{ai}(f)}{V_s(f)}\right|^2\right)$$

Source: Universal Chiplet Interconnect Express Consortium (UCIe™). Refer to the UCIe™ specification for additional info.

Channel Spec: VTF for Advanced Package

Table 5-11. Channel Characteristics

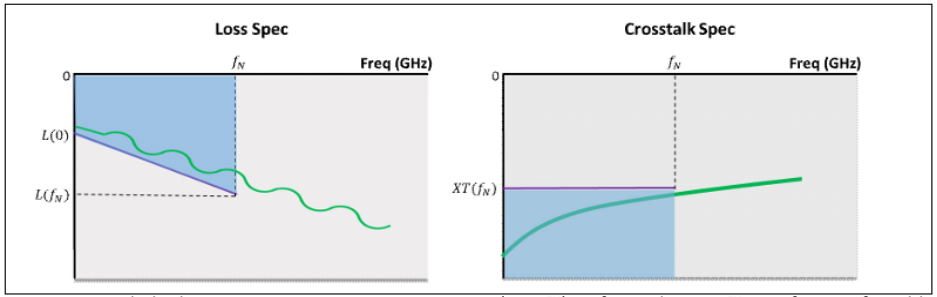
Data Rate	4-16 GT/s	24, 32 GT/s
VTF Loss (dB)	$L(f_N) > -3$	$L(f_N) > -5$
VTF Crosstalk (dB)[a]	$XT(f_N) < 1.5\ L(f_N) - 21.5$ and $XT(f_N) < -23$	$XT(f_N) < 1.5\ L(f_N) - 19$ and $XT(f_N) < -24$

a. Based on Voltage Transfer Function Method (Tx: 25 ohm / 0.25 pF; Rx: 0.2 pF).

f_N is the Nyquist frequency. The equations in the table form a segmented line in the loss-crosstalk coordinate plane, defining the pass/fail region.

Loss and crosstalk are specified by a mask defined by the $L(f_N)$ and $XT(f_N)$ at Nyquist frequency. It is a linear mask from DC to f_N for loss and flat mask for crosstalk, illustrated by Figure 5-18. Loss from DC to f_N needs to be above the spec line. Crosstalk from DC to f_N needs to be below the spec line. The green line in Figure 5-18 is a representative passing signal.

Figure 5-18. Loss and Crosstalk Mask



Source: Universal Chiplet Interconnect Express Consortium (UCIe™). Refer to the UCIe™ specification for additional info.

Channel Spec: VTF for Standard Package

5.7.3 Standard Package

Interconnect channel should be designed with 50 ohm characteristic impedance. Insertion loss and crosstalk for requirement at Nyquist frequency with Receiver termination is defined in Table 5-18.

Table 5-18. IL and Crosstalk for Standard Package: With Receiver Termination Enabled

Data Rate	4, 8 GT/s	12, 16 GT/s	24, 32 GT/s
VTF Loss (dB)[a b c]	$L(0) > -4.5$ $L(f_N) > -7.5$	$L(0) > -4.5$ $L(f_N) > -6.5$	$L(0) > -4.5$ $L(f_N) > -7.5$
VTF Crosstalk (dB)	$XT(f_N) < 3 * L(f_N) - 11.5$ and $XT(f_N) < -25$	$XT(f_N) < 3 * L(f_N) - 11.5$ and $XT(f_N) < -25$	$XT(f_N) < 2.5 * L(f_N) - 10$ and $XT(f_N) < -26$

a. Voltage Transfer Function for 4 GT/s and 8 GT/s (Tx: 30 ohm / 0.3pF; Rx: 50 ohm / 0.3pF).
b. Voltage Transfer Function for 12 GT/s and 16 GT/s (Tx: 30 ohm / 0.2pF; Rx: 50 ohm / 0.2pF).
c. Voltage Transfer Function for 24 GT/s and 32 GT/s (Tx: 30 ohm / 0.125pF; Rx: 50 ohm / 0.125pF).

IL and crosstalk for requirement at Nyquist frequency without Receiver termination is defined by Table 5-19. Loss and crosstalk specifications between DC and Nyquist f_N follow the same methodology defined in Section 5.7.2.1.

Table 5-19. IL and Crosstalk for Standard Package: No Rx Termination

Data Rate	4-12 GT/s	16 GT/s
VTF Loss (dB)[a b]	$L(f_N) > -1.25$	$L(f_N) > -1.15$
VTF Crosstalk (dB)	$XT(f_N) < 7 * L(f_N) - 12.5$ and $XT(f_N) < -15$	$XT(f_N) < 4 * L(f_N) - 13.5$ and $XT(f_N) < -17$

a. Voltage Transfer Function for 4 GT/s and 8 GT/s (Tx: 30 ohm / 0.3pF; Rx: 0.2 pF).
b. Voltage Transfer Function for 12 GT/s and 16 GT/s (Tx: 30 ohm / 0.2pF; Rx: 0.2 pF).

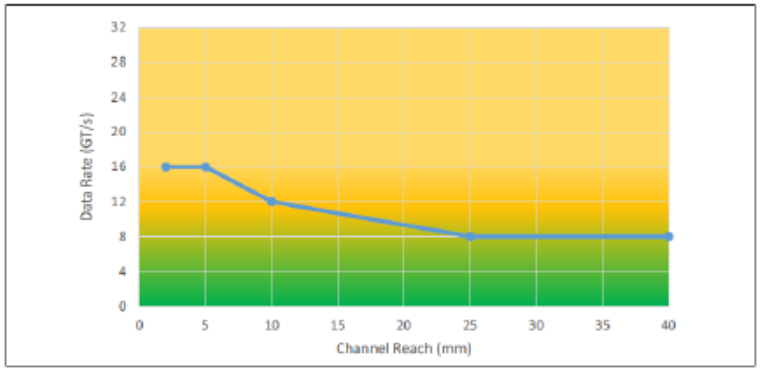
Source: Universal Chiplet Interconnect Express Consortium (UCIe™). Refer to the UCIe™ specification for additional info.

UCIe Routing/Signal Exit Order Requirement

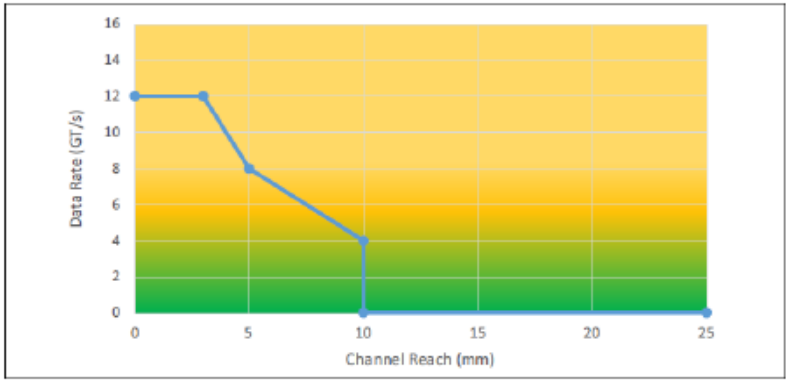
Maximum Channel reach for unterminated Receiver (TX swing = 0.85V)

Data Rate (GT/s)	Channel Reach (mm)
16	5
12	10
8 and below	All supported Lengths

Receiver termination map for Table 5-7 (TX Swing = 0.85 V)



Receiver Termination Map for Table 5-6 (Tx Swing = 0.4 V)

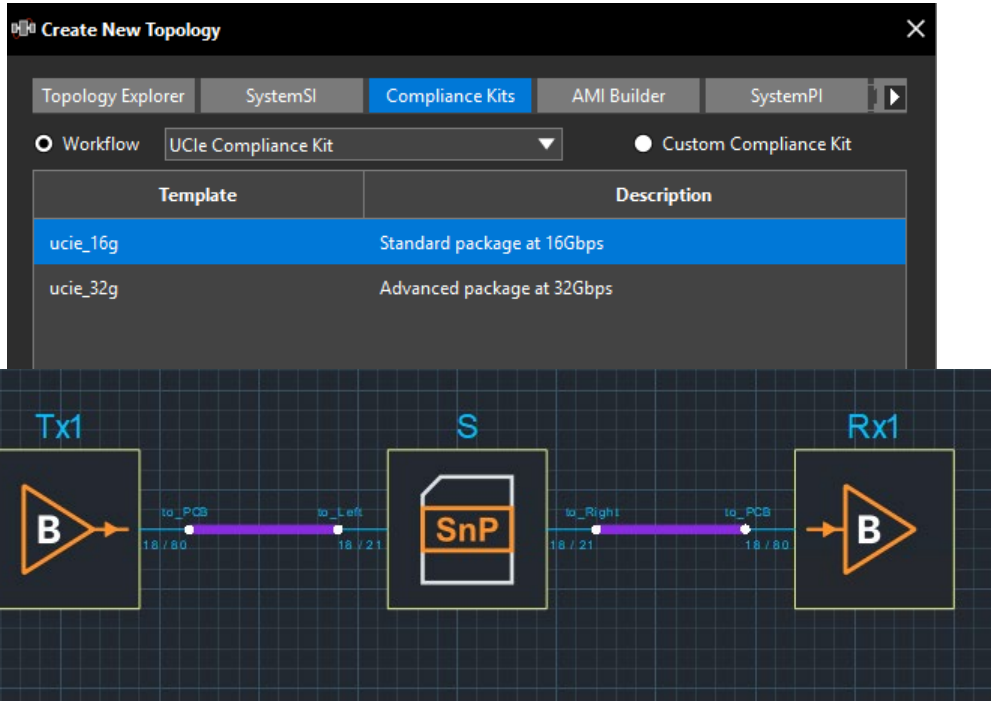


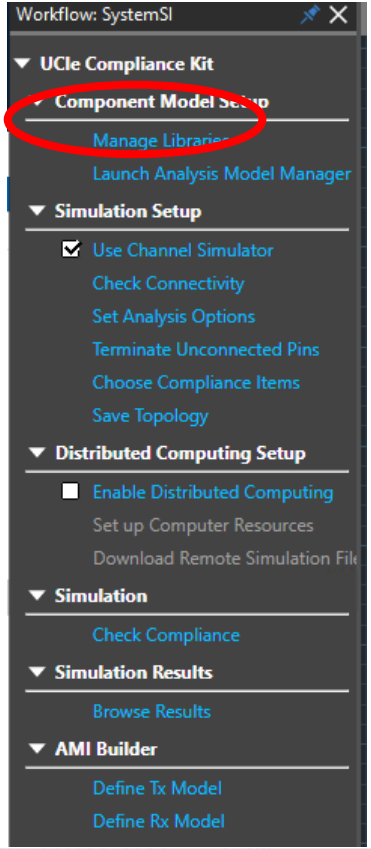
Source: Universal Chiplet Interconnect Express Consortium (UCIe™). Refer to the UCIe™ specification for additional info.

Compliance Kit

UCIe Interface Added in Compliance Kits

- Introduced new compliance kit for UCIe™ interface



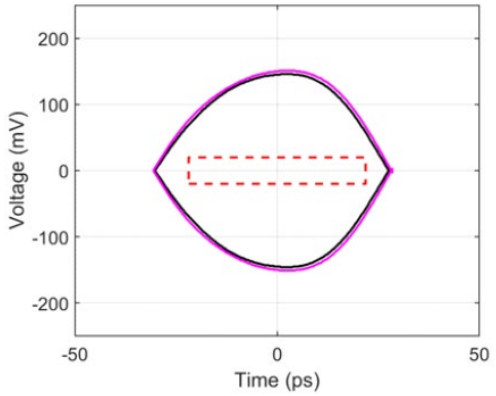


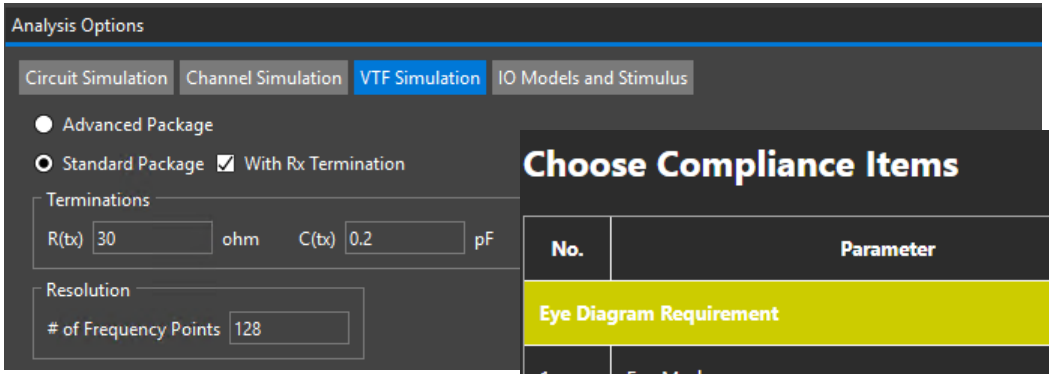
Details of the New UCIe Kit

- UCIe™ Spec v1.1
- Templates for data rates of 16 and 32Gbps
- Generic IBIS-AMI models
- Generic UCIe reference channel
- VTF calculations
- Compliance check report

Compliance Items

- As required in UCIe™ Spec
  - Eye mask
  - VTF





Choose Compliance Items

No.	Parameter	Values	☑
Eye Diagram Requirement			
1	Eye Mask	Eye Height = 40mV, Eye Width = 0.75UI	☑
Voltage Transfer Functions			
2	VTF Loss	L(0) > -4.5 and $L(f_N)$ > -6.5	☑
3	VTF Crosstalk	$XT(f_N) < 3*L(f_N) - 11.5$ and $XT(f_N) < -25$	

Compliance Checking

- Spec-based measurements

UCIe Compliance Report

Generated by Topology Workbench, Cadence Design Systems Inc.,
Aug 14, 2024

Useful Links

- **Cadence website:** http://www.cadence.com

General Information

- **Project File:** new_test.topx
- **Circuit Simulator:** SPDSIM

Summary of Results

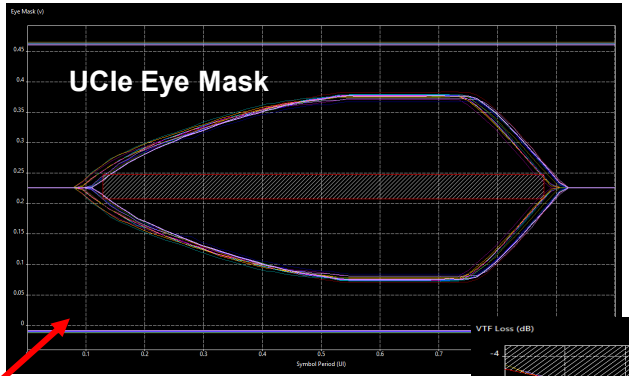
This report shows the results of the compliance testing using Cadence TopXp.
The channel simulated violates one or more compliance requirements.

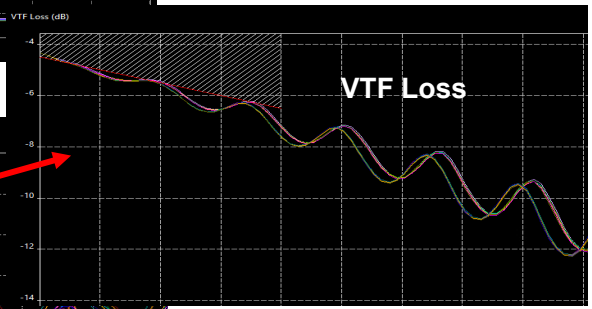
Eye Diagram Requirement

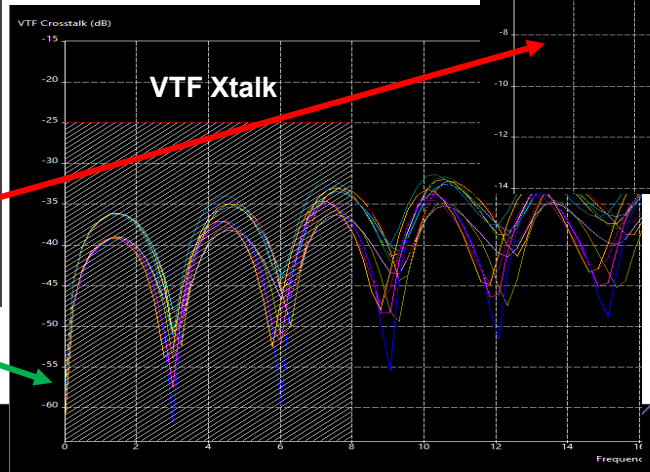
Item	Value	Simulation Results	Pass/Fail
Eye Mask	Eye Height = 40mV, Eye Width = 0.75UI	Eye Mask	Fail

Voltage Transfer Functions

Item	Value	Simulation Results	Pass/Fail
VTF Loss	L(0) > -4.5 and L(f_N) > -6.5	VTF Loss	Fail
VTF Crosstalk	XT(f_N) < 3*L(f_N) - 11.5 and XT(f_N) < -25	VTF Crosstalk	Pass

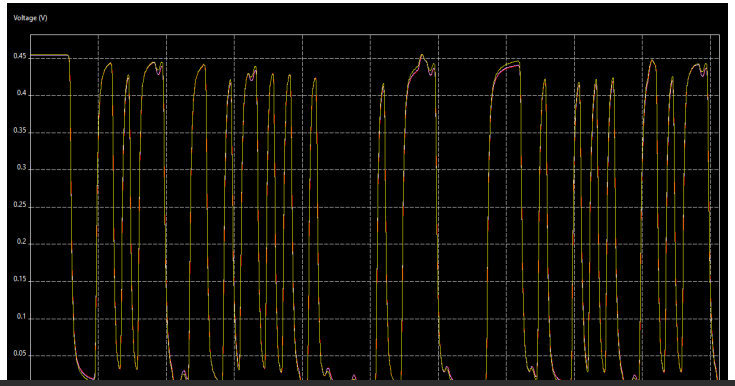


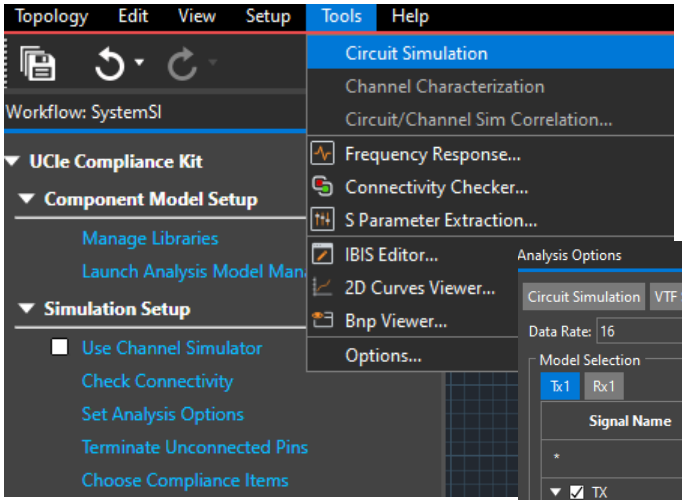


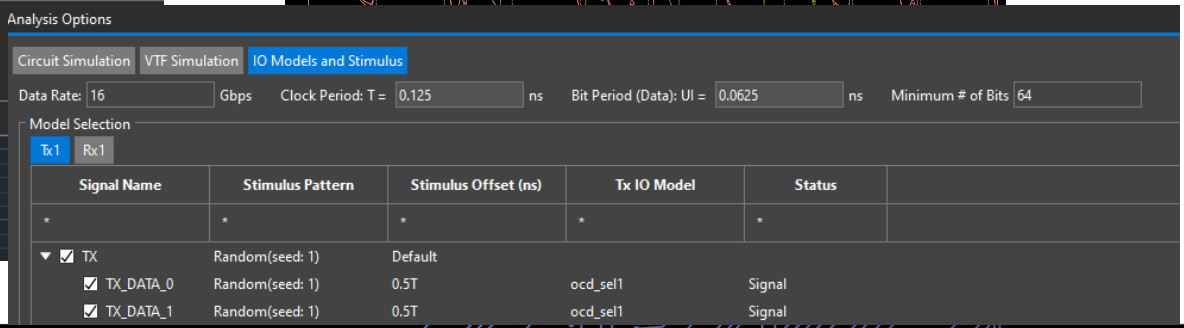


Running Transient Simulation (Circuit Simulation)

- You can directly run circuit simulation in the UCIe™ Compliance Kit flow
  - Checking signal and crosstalk

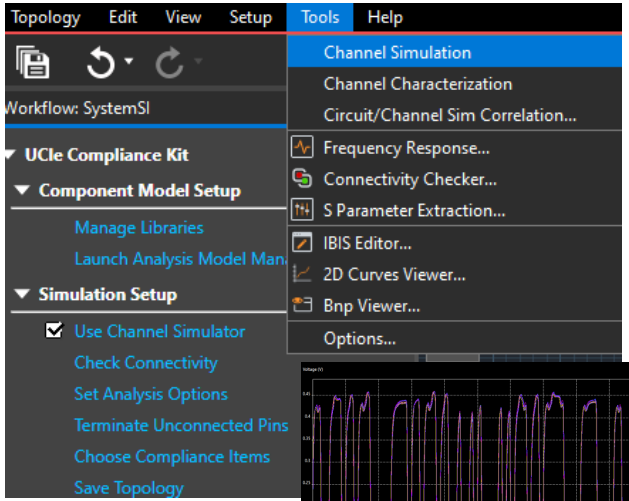


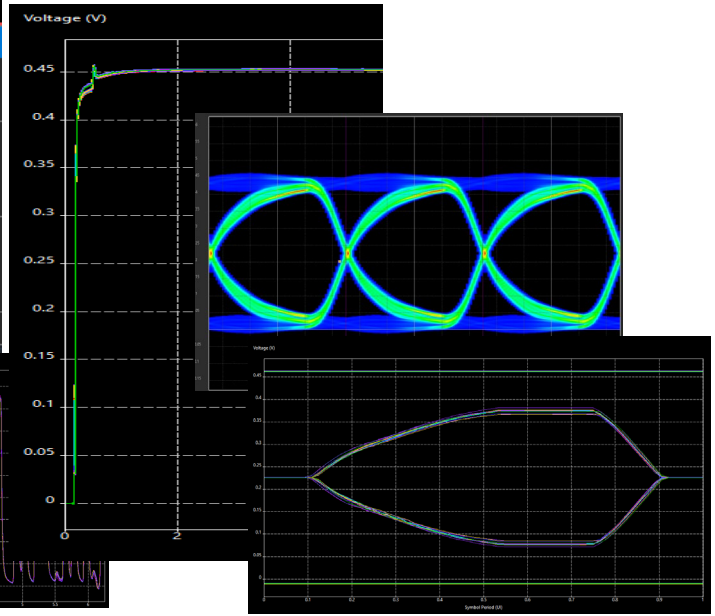




Running Channel Simulation

- You can run full channel simulation in the UCIe™ Compliance Kit flow



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Channel Report

Thu Nov 28 17:30:30 2024

General:

        Simulation Type          = Time Domain
        Data Rate                =  16 Gbps
        Number of Bits           = 9728
        Number of Eye Bits       = 1332
        Ignore Bits              = 8396
        Channel Coding           = No
        Primary Driver           = Tx1_TX_DATA_0
        Data Pattern             = random
        Number of signals in bus = 17
        Characterization Data    = C:\Users\zhenm\OneDrive - Cadence Design
        Characterization Type    = Even Mode Ramp Characterization


Jitter Inputs:

        Random Jitter            = 1 %

Noise Inputs:

        Random Noise             = 1 mV

Eye Contour Measurements:

        Eye Height               = 319 mV
        Eye Height Measured at   = 0.5 UI
        Eye Jitter               = 0.03 UI
        Eye Jitter Measured at   = 225 mV
        Eye Norm Jitter and Noise (NJN) = 0.49
        Channel Operating Margin (COM) = 18.92 dB

Channel Operating Margin (COM) at BER 1e-16  = 14.11 dB
Eye Density Signal to Noise Ratio (SNR)  = 105.30

BER Measurements:

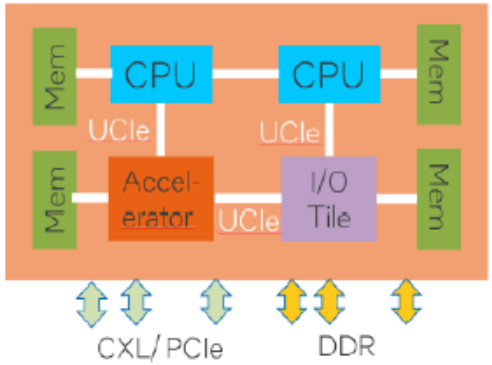
        LBER(log BER)            Eye Width(UI)
        -17                      0.78
        -16                      0.79
        -15                      0.80
        -14                      0.80
        -13                      0.81
        -12                      0.82
        -11                      0.82
        -10                      0.83
        -9                       0.84
        -8                       0.85
        -7                       0.86
        -6                       0.87
        -5                       0.88
        -4                       0.89
        -3                       0.90
```

Case Study

UCIe Chiplets and Packaging

- **UCIe–Chiplets Integration Challenges**
  - Complex Die-2-Die routes (Signal, Power)
  - Maintain Signal Exit orders at the beach front (die edge), while maintaining strict skew matching (lane-2-lane, lane-2-forwarded clocks,…)
  - Meet SI /PI budget for channel to ensure overall End-2-End (Interconnected die) performance requirements.
  - Mix of AP, SP PHYs, Term/Unterminated routes, varying die-2-die spacing , Performance in High/Low Swing modes.
  - VTF based channel analysis.

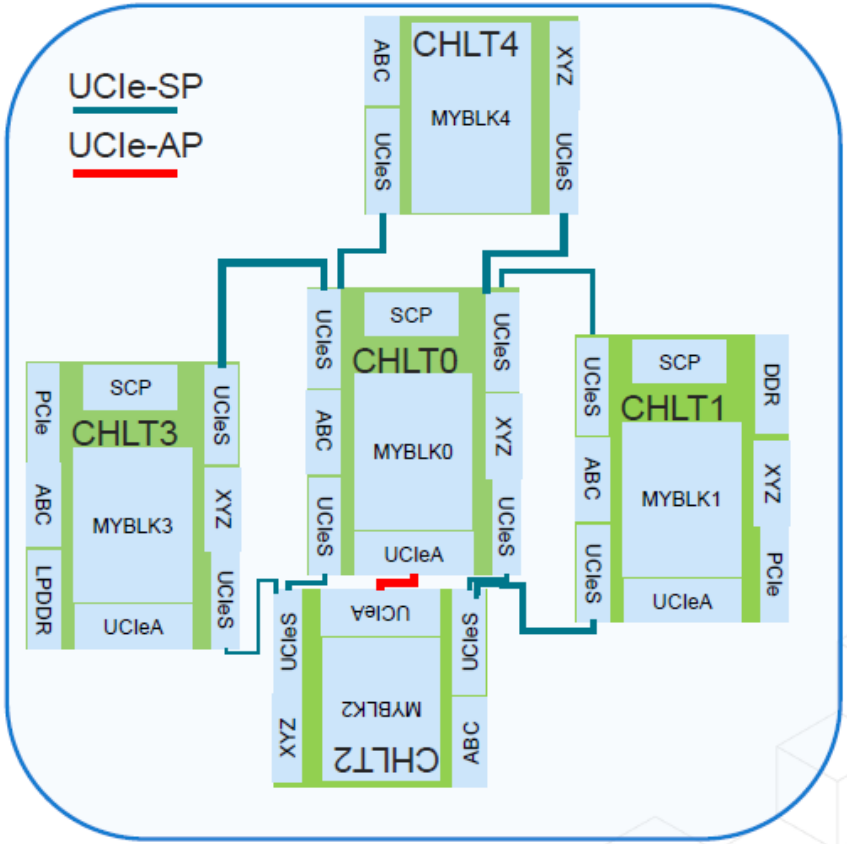
A Package Composed of CPU Dies, Accelerator Die(s), and I/O Tile Die Connected through UCIe



- **Need for UCIe-Centric Packaging Solutions**
  - A toolkit for Automating Package designs for UCIe based chiplet integration.

Chiplet Package Design – Die Placement/Routing

- Placement
  - Multiple chiplet instantiations UCIe-SP, UCIe-AP
  - Orientation and alignments
- Import models
  - Physical
  - IBIS
  - Rdie, Cdie, .pdn, current die model (.cdm)
- Choose channel (from PDK library)
  - Organic
  - CoWoS-S/R/L
  - Bridge interposer
  - …



UCIe Routing/Signal Exit Order Requirements

Figure 5-41. Standard Package x16 interface: Signal exit order

Layer 1	Tx	0	1	2	3	trk	vld	12	13	14	15	15	14	13	12	vld	trk	3	2	1	0	Rx
Layer 2	Module	4	5	6	7	ckp	ckn	8	9	10	11	11	10	9	8	ckn	ckp	7	6	5	4	Module
Sideband			txdatasb				txcksb								rxcksb				rxdatasb			

Figure 5-44. Standard Package cross section for stacked module

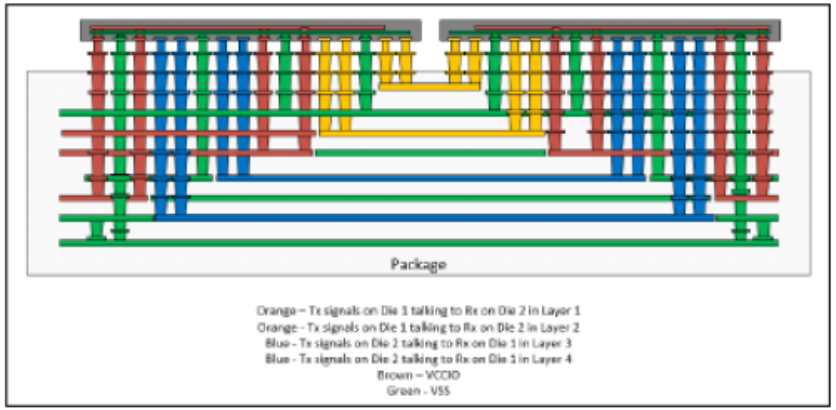


Figure 5-43. Standard Package x32 interface: Signal exit routing

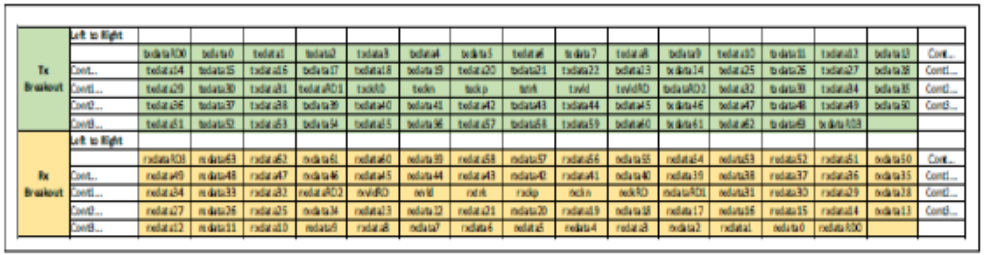
Layer 1	Tx	0	1	2	3	trk	vld	12	13	14	15	15	14	13	12	vld	trk	3	2	1	0	Rx
Layer 2	Module 1	4	5	6	7	ckp	ckn	8	9	10	11	11	10	9	8	ckn	ckp	7	6	5	4	Module 1
Layer 3	Rx	0	1	2	3	trk	vld	12	13	14	15	15	14	13	12	vld	trk	3	2	1	0	Tx
Layer 4	Module 2	4	5	6	7	ckp	ckn	8	9	10	11	11	10	9	8	ckn	ckp	7	6	5	4	Module 2
Sideband		m1txdatasb				m2rxdatasb		m1txcksb		m2rxcksb		m2txcksb		m1rxcksb		m2txdatasb			m1rxdatasb			Sideband

Source: Universal Chiplet Interconnect Express Consortium (UCIe™). Refer to the UCIe™ specification for additional info.

UCIe AP Interposer Design Requirements

Figure 5-23 shows the signal exit order for the 10-column x64 Advanced Package bump map.

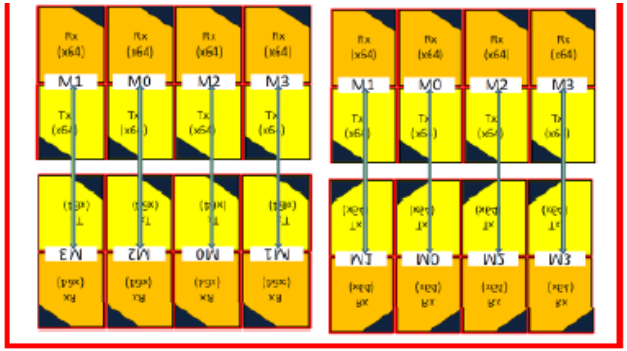
Figure 5-23. 10-column x64 Advanced Package Bump map: Signal exit order



- UCIe standard allocates 25% UI of jitter to channel related degradation (loss+xtalk)
- After UCIe data channels are designed on the interposer, the resulting design should be verified with circuit level simulations
- With an ideal driver and receiver circuit, using the interposer channel, the eye should have ≥ 75% UI horizontal opening and ≥ 40mV vertical height
- Example: at 16Gbps, channel related jitter (xtalk+loss) should be ≤ 15.6ps

- UCIe is sensitive to supply noise, recommend keeping the UCIe PHY supplies separate than the SoC supplies
- The AP UCIe PHY was designed with the assumption that there is a total of 50 mVpp supply noise, where 20-25mVpp of that being allocated to the IP.
- Using the die model for the IP in conjunction with the extracted interposer and package s-parameter models, **the target should be that the supply noise be less than 25mVpp**. Higher noise values will need to be evaluated on a case-by-case basis.
- Additionally, the IR drop across the interposer power routings should be minimized. We should target this drop to be less than 5mV, but there is some flexibility this depending on the domain

GUI-Based Link Connectivity



- Fixed signal connectivity between Die modules [link_AP.v, link_sp.v].
- Connect the Dies/ Links through Verilog File Placement in GUI. Validated Connectivity by Construction.
- Die placements / orientation (Die Rotate, Mirrored Die Rotate, Multi Modules)

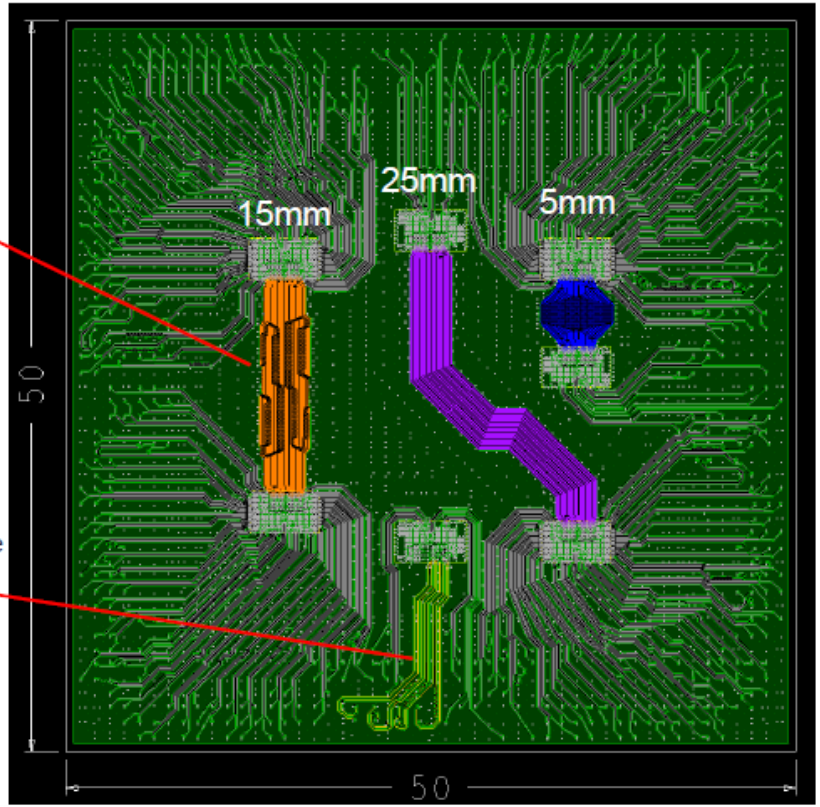
Die 0	Link SP	Die 1	Die 0	Link SP	Die 1
txclkp	→	rxclkp	rxclkp	←	txclkp
txclkn	→	rxclkn	rxclkn	←	txclkn
txdata0	→	rxdata0	rxdata0	←	txdata0
txdata1	→	rxdata1	rxdata1	←	txdata1
txdata2	→	rxdata2	rxdata2	←	txdata2
txdata3	→	rxdata3	rxdata3	←	txdata3
txdata4	→	rxdata4	rxdata4	←	txdata4
txdata5	→	rxdata5	rxdata5	←	txdata5
txdata6	→	rxdata6	rxdata6	←	txdata6
txdata7	→	rxdata7	rxdata7	←	txdata7
txdata8	→	rxdata8	rxdata8	←	txdata8
txdata9	→	rxdata9	rxdata9	←	txdata9
txdata10	→	rxdata10	rxdata10	←	txdata10
txdata11	→	rxdata11	rxdata11	←	txdata11
txdata12	→	rxdata12	rxdata12	←	txdata12
txdata13	→	rxdata13	rxdata13	←	txdata13
txdata14	→	rxdata14	rxdata14	←	txdata14
txdata15	→	rxdata15	rxdata15	←	txdata15
txvld	→	rxvld	rxvld	←	txvld
txtrk	→	rxtrk	rxtrk	←	txtrk
txdatasb	→	rxdatasb	rxdatasb	←	txdatasb
txclksb	→	rxclksb	rxclksb	←	txclksb

link_SP.v

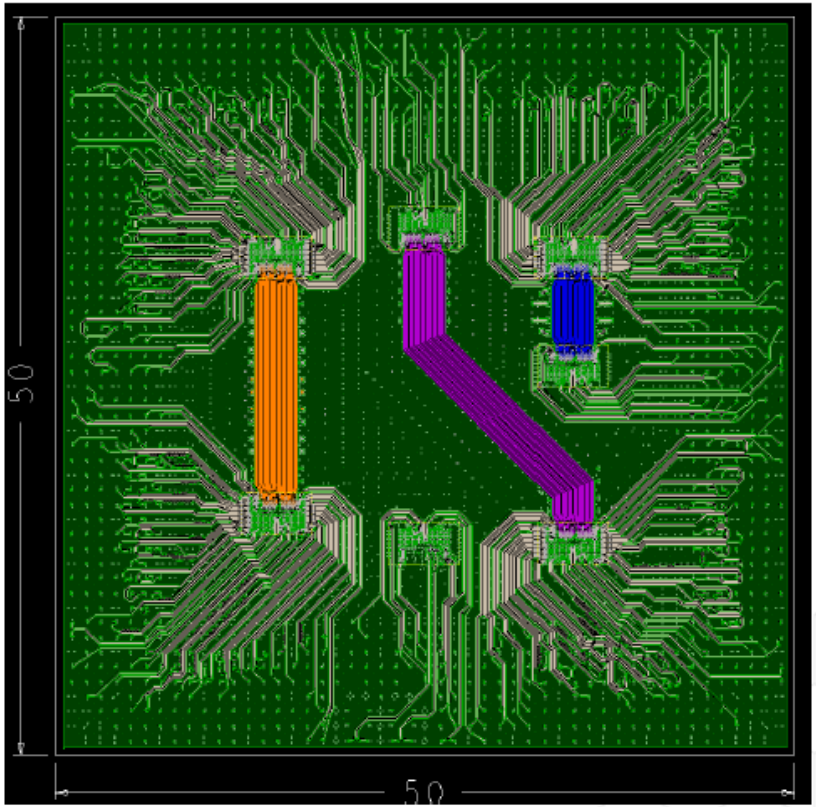
Die 0	Link AP	Die 1	Die 0	Link AP	Die 1
txclkp	→	rxclkp	rxclkp	←	txclkp
txclkn	→	rxclkn	rxclkn	←	txclkn
txdata0	→	rxdata0	rxdata0	←	txdata0
txdata1	→	rxdata1	rxdata1	←	txdata1
txdata2	→	rxdata2	rxdata2	←	txdata2
txdata3	→	rxdata3	rxdata3	←	txdata3
txdata4	→	rxdata4	rxdata4	←	txdata4
txdata5	→	rxdata5	rxdata5	←	txdata5
...	→	...	...	←	...
...	→	...	...	←	...
...	→	...	...	←	...
...	→	...	...	←	...
txdata58	→	rxdata58	txdata58	←	rxdata58
txdata59	→	rxdata59	txdata59	←	rxdata59
txdata60	→	rxdata60	txdata60	←	rxdata60
txdata61	→	rxdata61	txdata61	←	rxdata61
txdata62	→	rxdata62	txdata62	←	rxdata62
txdata63	→	rxdata63	txdata63	←	rxdata63
txvld	→	rxvld	rxvld	←	txvld
txtrk	→	rxtrk	rxtrk	←	txtrk
txdataRD0	→	rxdataRD0	rxdataRD0	←	txdataRD0
txdataRD1	→	rxdataRD1	rxdataRD1	←	txdataRD1
txdataRD2	→	rxdataRD2	rxdataRD2	←	txdataRD2
txdataRD3	→	rxdataRD3	rxdataRD3	←	txdataRD3
txvldRD	→	rxvldRD	rxvldRD	←	txvldRD
txtrkRD	→	rtrkRD	rtrkRD	←	txtrkRD
txdatasb	→	rxdatasb	rxdatasb	←	txdatasb
txclksb	→	rxclksb	rxclksb	←	txclksb
txdatasbRD	→	rxdatasbRD	rxdatasbRD	←	txdatasbRD
txclksbRD	→	rxclksbRD	rxclksbRD	←	txclksbRD

- Complete non-Die2-Die , Power Rail connectivity.

Blizzard N7 SP – Package Overview



Layer 2 Routing



Layer 4 Routing

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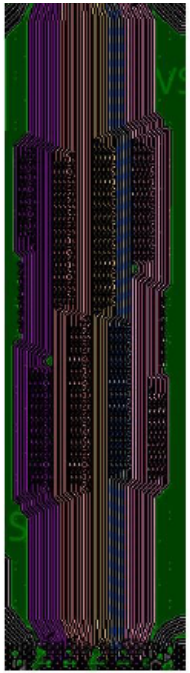
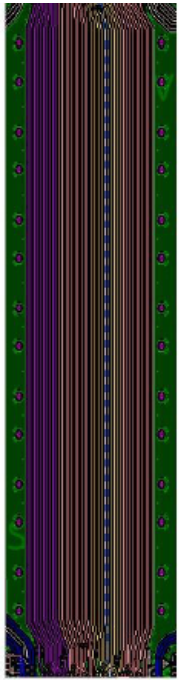
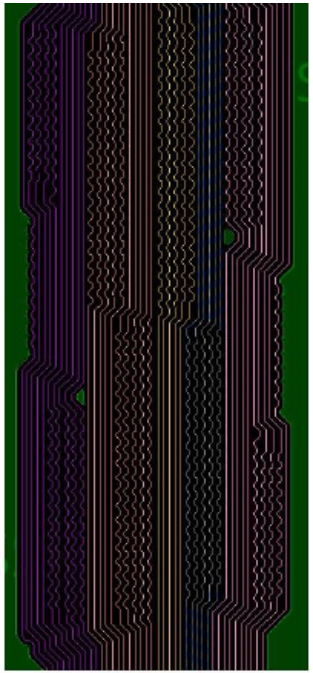
SP - Routing (16mm average) Samples and Matching Lane Skews



Layer 2



Layer 4



Layer 2 - Zoom Version

			(mm)	(ps)	delta	
1	Layer 6	RXCKSB_M0_AB	16.83	89.04	0.1	
2		RXDATASB_M0_AB	16.81	88.94		
3	Layer 4	RXDATA10_M0_AB	16.27	84.34	0.38	3.84
4		RXDATA6_M0_AB	16.25	84.24		
5		RXDATA5_M0_AB	16.24	84.2		
6		RXDATA11_M0_AB	16.24	84.19		
7		RXDATA9_M0_AB	16.23	84.15		
8		RXDATA7_M0_AB	16.23	84.12		
9		RXDATA4_M0_AB	16.22	84.07		
10		RXDATA8_M0_AB	16.22	84.06		
11		RXCKN_M0_AB	16.20	83.96		
12		RXCKP_M0_AB	16.20	83.96		
13	Layer 2	RXDATA0_M0_AB	15.98	80.63	0.13	
14		RXDATA14_M0_AB	15.98	80.61		
15		RXDATA12_M0_AB	15.98	80.61		
16		RXDATA3_M0_AB	15.97	80.61		
17		RXDATA13_M0_AB	15.97	80.6		
18		RXVLD_M0_AB	15.97	80.58		
19		RXDATA1_M0_AB	15.97	80.58		
20		RXTRK_M0_AB	15.97	80.58		
21		RXDATA2_M0_AB	15.96	80.56		
22		RXDATA15_M0_AB	15.96	80.5		

- 16 x 2 – 32 ports for Rx to Tx Data lanes
- 4 x 2 - 8 ports for Clock, TRK & VLD
- 7 x 2 – 14 ports for VDD Core Power.

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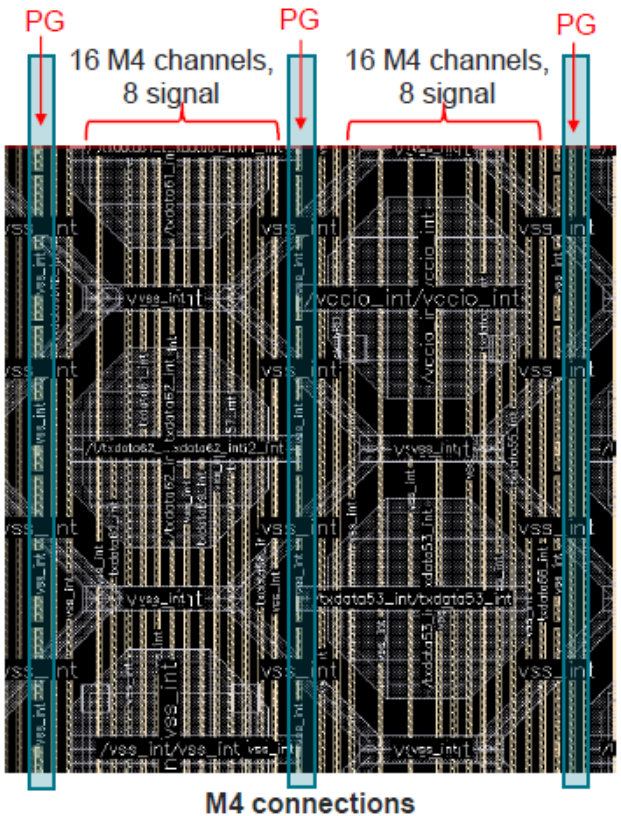
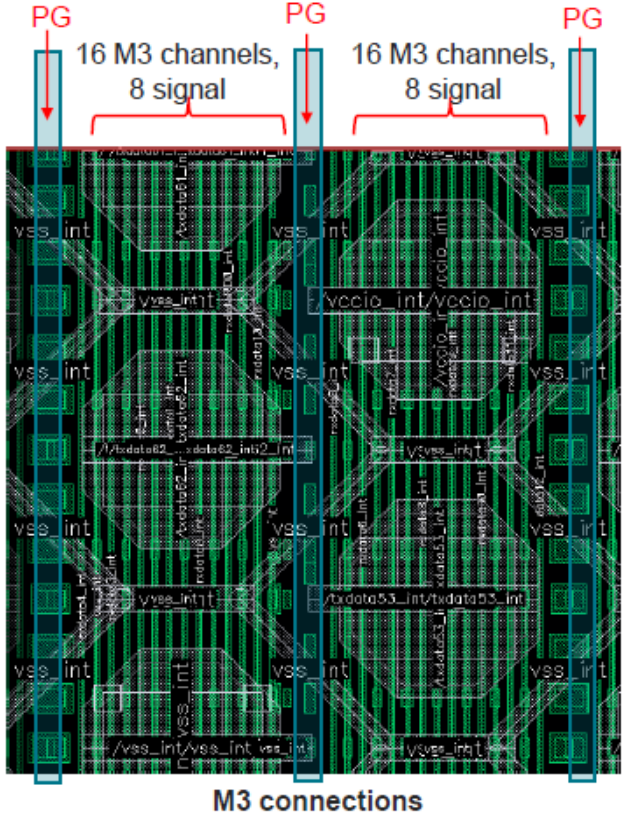
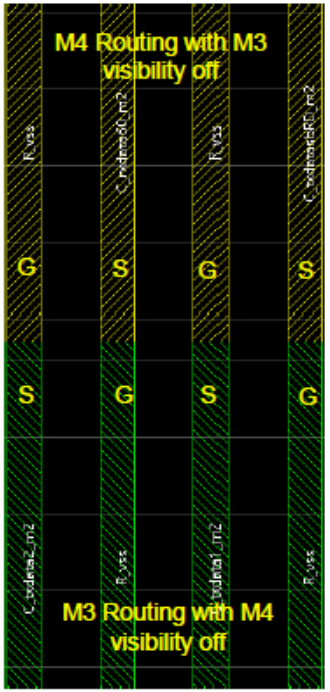
M4 – M3 Metal Connections – Sample – CoWos_S



M4 connections



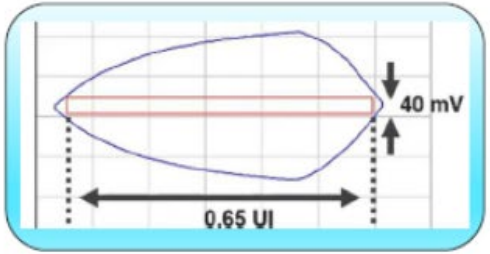
M3 connections



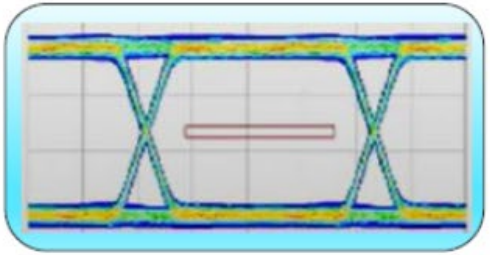
Staggered Pattern

Pattern:
M3: SGSG
M4: GSGS

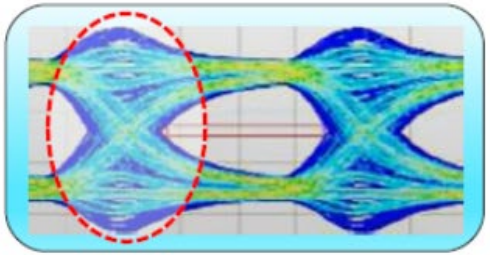
Die2Die Route - Samples



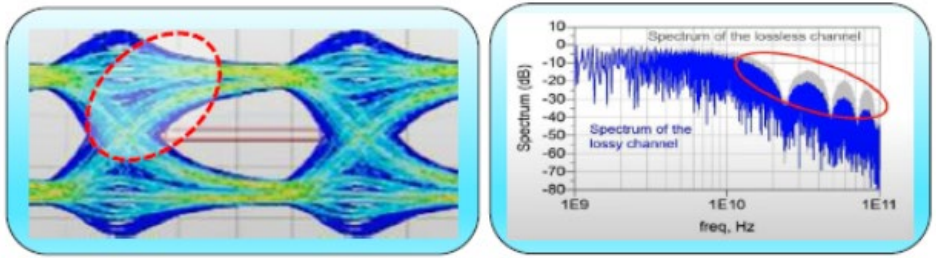
Simulate noiseless, jitter-less behavioral Tx and Rx models for ideal eye mask at receiver



Thick eye level – Near-end crosstalk – Traces are closer



Far-end crosstalk – closes Rx eye undershoot/overshoot



Simulate noiseless, jitter-less behavioral Tx and Rx models for ideal eye mask at receiver

Optimize trace spacing – to meet UCIe™ VTF crosstalk specification, open the eye (meet eye mask spec)

Die2Die Signal Integrity Checks

- Simulate noiseless, jitter-less behavioral Tx and Rx models for ideal eye mask compliance at receiver
  - To optimize the channel routes
- Channel crosstalk, jitter analysis
- Frequency-dependent loss (Tx and Rx channels)
- Analysis conditions:
  - Rx eye analysis for terminated/unterminated use cases – SP
  - AP links unterminated
  - Analysis with 45 Ohms < Rx termination < 55 Ohms
  - 0.4V < Tx swing < 0.85V
  - Support for all supported data rates
  - Support for IP – Process corners
  - Forwarded Rx clock phases: (90, 270), (45, 135)
- Signal analysis methods
  - Tx eye diagram analysis
  - VTF loss (for channel)

UCIe Toolkit Flow (Package Design, Analysis, Release)

UCIe™ Compliance Design Toolkit with a GUI front end for:

- Chiplet design import, placement
- Substrate/interposer – PDK – import
- Chiplet signal interconnects, package I/O connectivity
- Power domain design
- Lossless channel simulation for signal route strategies

3D – Extraction/S-parameter model generation
VTF model creation
Automated flow from routing>extraction>SI/PI
Iterate fixes, extraction, and SI analysis for review
Through meeting the Link requirement

Design/analysis interations to automate the toolkit

Demo

Please visit the Cadence Booth #827 for a Live Demo of the UCIe Compliance Kit